AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. - 6. (Canceled)

7. (Currently Amended) A power semiconductor module, comprising:

an electrically insulating substrate;

a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;

at least one semiconductor power chip mounted on said first electrically conductive layer;

a first electrically insulating material disposed between said electrically insulating substrate and said first electrically conductive layer and in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;

a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material;

wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by

said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped.

8. (Previously Presented) The power semiconductor module as claimed in claim 7, wherein the electrically insulating substrate is mounted on a bottom plate.

9. (Previously Presented) The power semiconductor module as claimed in claim 7, wherein at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate; and wherein a third insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral bottom region of the electrically insulating substrate.

10. (Previously Presented) The power semiconductor module as claimed in claim 7, wherein a rigid layer of resin is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material.

11. (Previously Presented) The power semiconductor module as claimed in claim 8, wherein at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate; and wherein a third

insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral bottom region of the electrically insulating substrate

12. (Previously Presented) The power semiconductor module as claimed in claim 11, wherein a rigid layer of resin is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material.

13. (Previously Presented) A power semiconductor module comprising:

an electrically insulating substrate;

a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;

at least one semiconductor power chip mounted on said first electrically conductive layer;

a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;

a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material;

wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by

said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped,

wherein the first electrically insulating material fills gaps in a junction between the first electrically conductive layer and said electrically insulating substrate.

14. (Previously Presented) A power semiconductor module, comprising:

an electrically insulating substrate;

a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;

at least one semiconductor power chip mounted on said first electrically conductive layer;

a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;

a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material,

wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped,

wherein at least one second electrically conductive layer is disposed between the bottom plate and at least one portion of a bottom surface of the electrically

insulating substrate, so as to selectively expose at least one peripheral bottom region of the electrically insulating substrate, and

wherein a third insulating material is disposed in a second corner formed by the second electrically conductive layer and the peripheral bottom region of the electrically insulating substrate.

15. (Previously Presented) A power semiconductor module, comprising:

an electrically insulating substrate;

a first electrically conductive layer disposed on at least one portion of a top surface of said electrically insulating substrate, so as to selectively expose at least one peripheral top region of said electrically insulating substrate;

at least one semiconductor power chip mounted on said first electrically conductive layer;

a first electrically insulating material disposed in a corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate;

a second insulating material at least partially embedding said semiconductor power chip, said electrically insulating substrate, said first electrically conductive layer, and said first electrically insulating material,

wherein the first electrically insulating material is a polyimide, and the surface of the first electrically insulating material disposed in the corner region formed by said first electrically conductive layer and said peripheral region of said electrically insulating substrate is concave-shaped, and

wherein a rigid layer of resin is provided between the second electrically insulating material and the semiconductor chip, the substrate, the first conductive layer and the first electrically insulating material.

16. (Previously Presented) The power semiconductor module as claimed in claim 7, wherein the first electrically insulating material has a low viscosity.

17. (Previously Presented) The power semiconductor module as claimed in claim 16, wherein the first electrically insulating material has a viscosity v such that $v \leq 1.0$ Pa·s.

18. (Previously Presented) The power semiconductor module as claimed in claim 13, wherein the first electrically insulating material has a low viscosity.

19. (Previously Presented) The power semiconductor module as claimed in claim 18, wherein the first electrically insulating material has a viscosity v such that $v \leq 1.0$ Pa·s.